Applicant: Hidetoshi Nishikawa Attorney's Docket No.: 19415-005US1 / PCT-04R-Serial No.: 10/561,552 155/US

Filed : March 20, 2006

Page : 2 of 14

Amendments to the Specification:

Please replace the paragraph beginning at page 7, line 1 with the following <u>amended</u> paragraph:

-- Fig. 11 is a circuit diagram showing the configuration of a conventional output buffer circuit; [[and]] --

Please replace the paragraph beginning at page 7, line 3 with the following <u>amended</u> paragraph:

-- Fig. 12 is a circuit diagram showing the configuration of the transistor switch provided in the output buffer circuit of Fig. 11;[[.]] --

Please add the following new paragraphs after the paragraph ending at page 7, line 4:

- -- FIG. 13 is a schematic diagram showing the configuration of the transistor of the output circuit of the first embodiment;
- FIG. 14 is a schematic diagram showing another configuration of the transistor of the output buffer circuit of the first embodiment;
- FIG. 15 is a schematic diagram showing the configuration of the transistor of the output circuit of the first embodiment;
- FIG. 16 is a schematic diagram showing another configuration of the transistor of the output buffer circuit of the first embodiment;
- FIG. 17 is a circuit diagram showing another configuration of the output buffer circuit of the first embodiment;
- FIG. 18 is a circuit block diagram showing another configuration of the semiconductor integrated circuit device provided with the output buffer circuit of the first embodiment;
- FIG. 19 is a schematic diagram showing the configuration of the transistor of the output buffer circuit of the second embodiment;

Attorney's Docket No.: 19415-005US1 / PCT-04R-155/US

Applicant : Hidetoshi Nishikawa Serial No. : 10/561,552 Filed : March 20, 2006

Page : 3 of 14

FIG. 20 is a schematic diagram showing another configuration of the transistor of the output buffer circuit of the second embodiment;

FIG. 21 is a schematic diagram showing another configuration of the output buffer circuit of the second embodiment; and

FIG. 22 is a circuit block diagram showing another configuration of the semiconductor integrated circuit device provided with the output buffer circuit of the second embodiment. --